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HARRIS Semiconductor

IRF9230, IRF9231, IRF9232, IRF9233

-5.5A and -6.5A, -150V and -200V, 0.8 and 1.2 Ohm, P-Channel Power MOSFETs

January 1998

Features

- **-5.5A and -6.5A, -150V and -200V**
- **$r_{DS(ON)}$ = 0.8Ω and 1.2Ω**
- **Single Pulse Avalanche Energy Rated**
- **SOA is Power Dissipation Limited**
- **Nanosecond Switching Speeds**
- **Linear Transfer Characteristics**
- **High Input Impedance**
- **Related Literature**
  - **TB334, "Guidelines for Soldering Surface Mount Components to PC Boards"**

Ordering Information

PART NUMBER	PACKAGE	BRAND
IRF9230	TO-204AA	IRF9230
IRF9231	TO-204AA	IRF9231
IRF9232	TO-204AA	IRF9232
IRF9233	TO-204AA	IRF9233

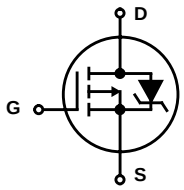
NOTE: When ordering, use the entire part number.

Description

These devices are P-Channel enhancement mode silicon gate power field effect transistors. They are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. All of these power MOSFETs are designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high power bipolar switching transistors requiring high speed and low gate drive power. These types can be operated directly from integrated circuits.

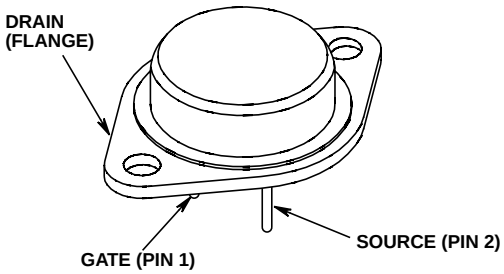
Formerly Developmental type TA17512.

Symbol



Packaging

JEDEC TO-204AA



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper ESD Handling Procedures.

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File Number **2226.1**

Absolute Maximum Ratings $T_C = 25^oC$, Unless Otherwise Specified

	IRF9230	IRF9231	IRF9232	IRF9233	UNITS
Drain to Source Breakdown Voltage (Note 1) V_{DS}	-200	-150	-200	-150	V
Drain to Gate Voltage (R_{GS} = 20kΩ) (Note 1) V_{DGRVGS}	-200	-150	-200	-150	V
Continuous Drain Current I_D	-6.5	-6.5	-5.5	-5.5	A
$T_C = 100^oC$ I_D	-4.0	-4.0	-3.5	-3.5	A
Pulsed Drain Current (Note 3) I_{DM}	-26	-26	-22	-22	A
Gate to Source Voltage V_{GS}	±20	±20	±20	±20	V
Maximum Power Dissipation P_D	75	75	75	75	W
Linear Derating Factor	0.6	0.6	0.6	0.6	$W/^oC$
Single Pulse Avalanche Energy Rating (Note 4) E_{AS}	500	500	500	500	mJ
Operating and Storage Temperature T_J, T_{STG}	-55 to 150	-55 to 150	-55 to 150	-55 to 150	^oC
Maximum Temperature for Soldering					
Leads at 0.063in (1.6mm) from Case for 10s T_L	300	300	300	300	^oC
Package Body for 10s, See Techbrief 334 T_{pkg}	260	260	260	260	^oC

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

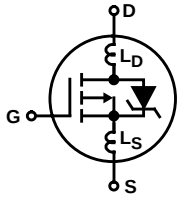
NOTE:

1. $T_J = 25^oC$ to $T_J = 125^oC$.

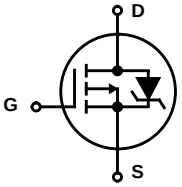
Electrical Specifications $T_C = 25^oC$, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Drain to Source Breakdown Voltage	BV_{DSS}	I_D = -250μA, V_{GS} = 0V, (Figure10)				
IRF9230, IRF9232			-200	-	-	V
IRF9231, IRF9233			-150	-	-	V
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}$, I_D = -250μA	-2	-	-4	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = Rated BV_{DSS}, V_{GS} = 0V	-	-	-25	μA
		V_{DS} = 0.8 x Rated BV_{DSS}, V_{GS} = 0V, $T_C = 125^oC$	-	-	-250	μA
On-State Drain Current (Note 2)	$I_{D(ON)}$	$V_{DS} > I_{D(ON)} \times r_{DS(ON)\ MAX}$, V_{GS} = -10V, (Figure 7)				
IRF9230, IRF9231			-6.5	-	-	A
IRF9232, IRF9233			-5.5	-	-	A
Gate to Source Leakage Current	I_{GSS}	V_{GS} = ±20V	-	-	±100	nA
Drain to Source On Resistance (Note 2)	$r_{DS(ON)}$	I_D = -3.5A, V_{GS} = -10V, (Figures 8, 9)				
IRF9230, IRF9231			-	0.5	0.8	Ω
IRF9232, IRF9233			-	0.8	1.2	Ω
Forward Transconductance (Note 2)	g_{fs}	$V_{DS} > I_{D(ON)} \times r_{DS(ON)\ MAX}$, I_D = -3.5A, (Figure 12)	2.2	3.5	-	S
Turn-On Delay Time	$t_{d(ON)}$	V_{DD} = 0.5 x Rated BV_{DSS}, $I_D \approx$ -6.5A, R_G = 50Ω, V_{GS} = -10V, (Figure 17, 18) R_L = 14.7Ω for V_{DSS} = 200V R_L = 10.9Ω for V_{DSS} = 150V MOSFET Switching Times are Essentially Independent of Operating Temperature	-	30	50	ns
Rise Time	t_r		-	50	100	ns
Turn-Off Delay Time	$t_{d(OFF)}$		-	50	100	ns
Fall Time	t_f		-	40	80	ns
Total Gate Charge (Gate to Source + Gate to Drain)	$Q_{g(TOT)}$	V_{GS} = -10V, I_D = -6.5A, V_{DS} = 0.8 x Rated BV_{DSS}, (Figures 14, 19, 20) Gate Charge is Essentially Independent of Operating Temperature	-	31	45	nC
Gate to Source Charge	Q_{gs}		-	18	-	nC
Gate to Drain "Miller" Charge	Q_{gd}		-	13	-	nC

Electrical Specifications $T_C = 25^oC$, Unless Otherwise Specified **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNITS
Input Capacitance	C_{ISS}	V_{DS} = -25V, V_{GS} = 0V, f = 1MHz, (Figure 11)		-	550	-	pF
Output Capacitance	C_{OSS}			-	170	-	pF
Reverse Transfer Capacitance	C_{RSS}			-	50	-	pF
Internal Drain Inductance	L_D	Measured Between the Contact Screw on the Flange that is Closer to Source and Gate Pins and the Center of Die	Modified MOSFET Symbol Showing the Internal Devices Inductances 	-	5.0	-	nH
Internal Source Inductance	L_S	Measured From the Source Lead, 6mm (0.25in) From the Flange and the Source Bonding Pad		-	12.5	-	nH
Thermal Resistance Junction to Case	$R_{\theta JC}$			-	-	1.67	$^oC/W$
Thermal Resistance Junction to Ambient	$R_{\theta JA}$	Typical Socket Mount		-	-	60	$^oC/W$

Source to Drain Diode Specifications

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNITS
Continuous Source to Drain Current	I_{SD}	Modified MOSFET Symbol Showing the Integral Reverse P-N Junction Diode		-	-	-6.5	A
Pulse Source to Drain Current (Note 3)	I_{SDM}			-	-	-26	A
Source to Drain Diode Voltage (Note 2)	V_{SD}	$T_C = 25^oC$, I_{SD} = -6.5A, V_{GS} = 0V, (Figure 13)		-	-	-1.5	V
Reverse Recovery Time	t_{rr}	$T_J = 150^oC$, I_{SD} = -6.5A, dI_{SD}/dt = 100A/µs		-	400	-	ns
Reverse Recovery Charge	Q_{RR}	$T_J = 150^oC$, I_{SD} = -6.5A, dI_{SD}/dt = 100A/µs		-	2.6	-	µC

NOTES:

2. Pulse test: pulse width ≤ 300µs, duty cycle ≤ 2%.
3. Repetitive rating: pulse width limited by maximum junction temperature. See Transient Thermal Impedance curve (Figure 3).
4. V_{DD} = 50V, starting $T_J = 25^oC$, L = 17.75mH, $R_G = 25\Omega$, peak I_{AS} = 6.5A (Figures 15, 16).

Typical Performance Curves Unless Otherwise Specified

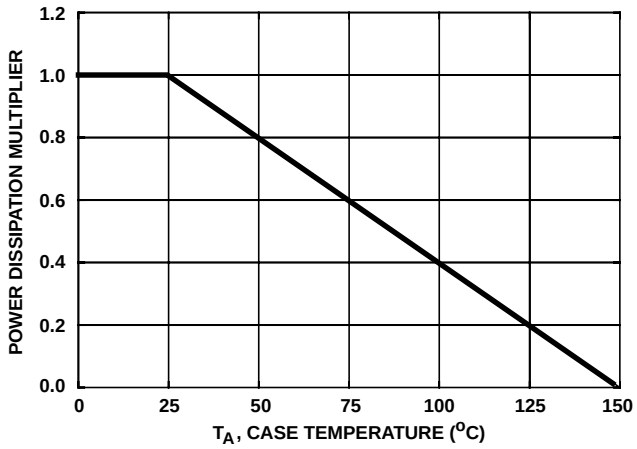


FIGURE 1. NORMALIZED POWER DISSIPATION vs CASE TEMPERATURE

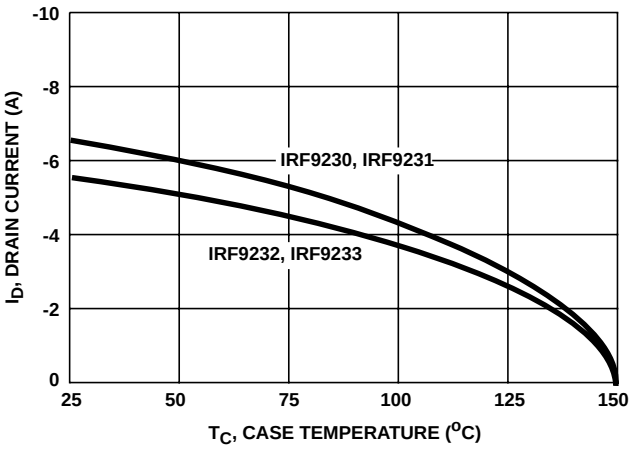


FIGURE 2. MAXIMUM CONTINUOUS DRAIN CURRENT vs CASE TEMPERATURE

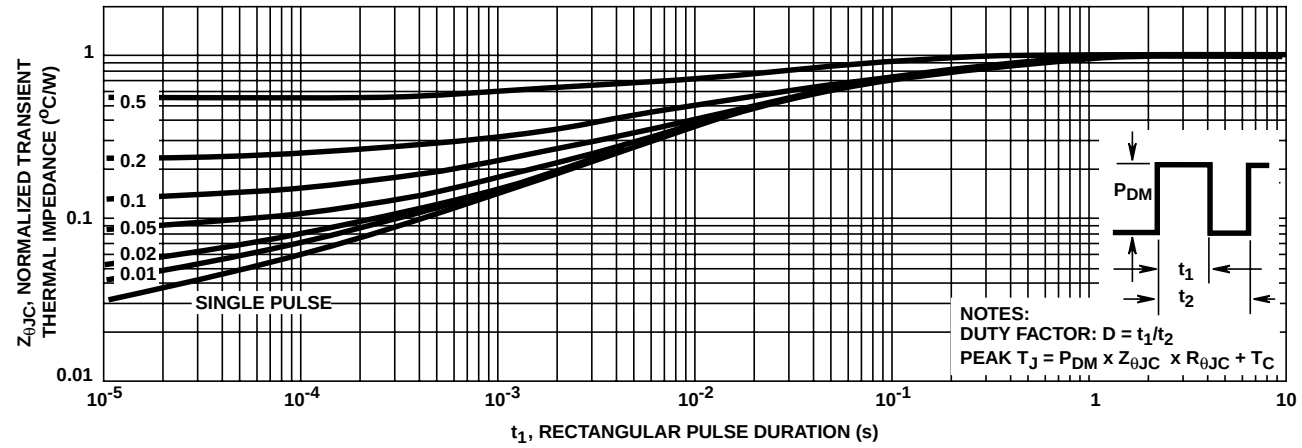


FIGURE 3. NORMALIZED MAXIMUM TRANSIENT THERMAL IMPEDANCE

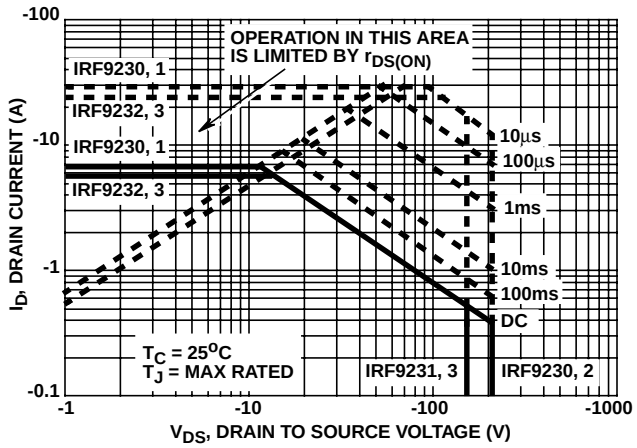


FIGURE 4. FORWARD BIAS SAFE OPERATING AREA

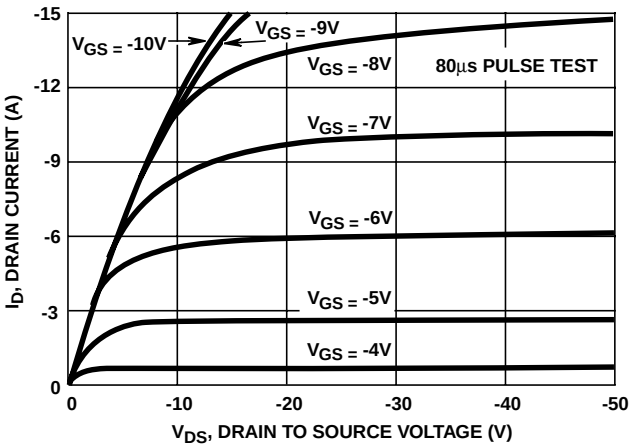


FIGURE 5. OUTPUT CHARACTERISTICS

Typical Performance Curves Unless Otherwise Specified (Continued)

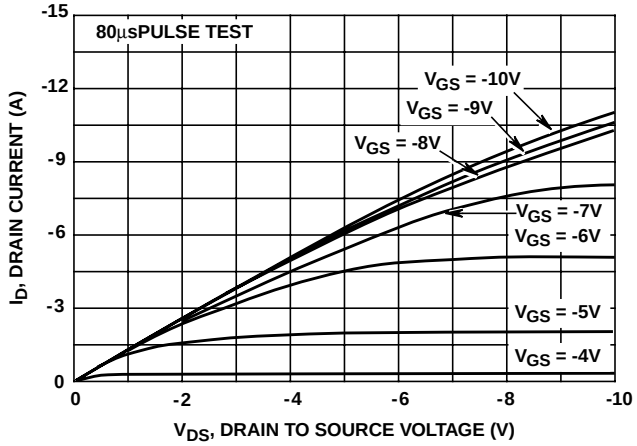


FIGURE 6. SATURATION CHARACTERISTICS

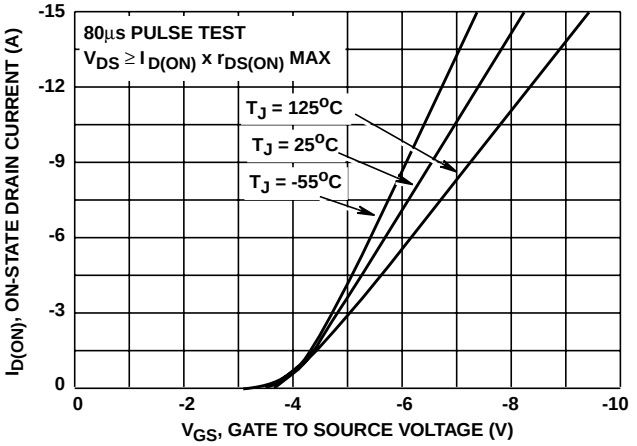
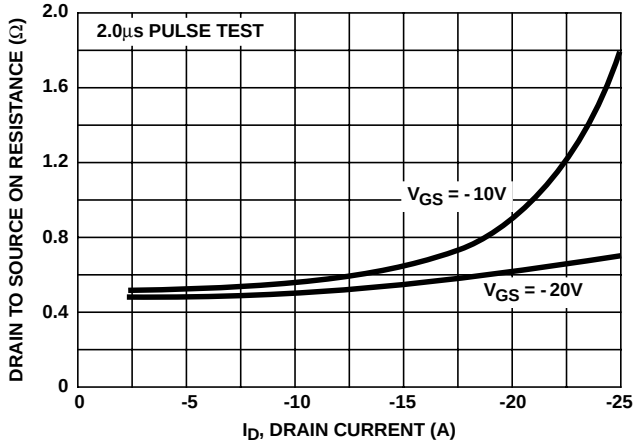


FIGURE 7. TRANSFER CHARACTERISTICS



NOTE: Heating effect of 2μs pulse is minimal.

FIGURE 8. DRAIN TO SOURCE ON RESISTANCE vs GATE VOLTAGE AND DRAIN CURRENT

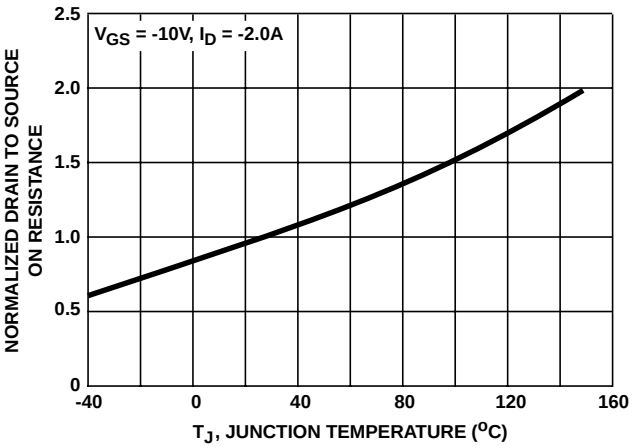


FIGURE 9. NORMALIZED DRAIN TO SOURCE ON RESISTANCE vs JUNCTION TEMPERATURE

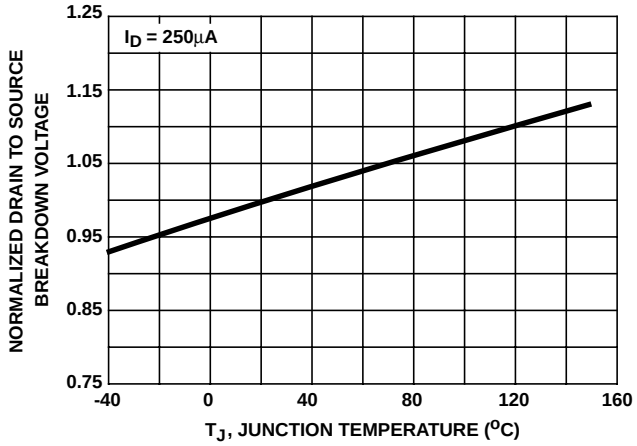


FIGURE 10. NORMALIZED DRAIN TO SOURCE BREAKDOWN VOLTAGE vs JUNCTION TEMPERATURE

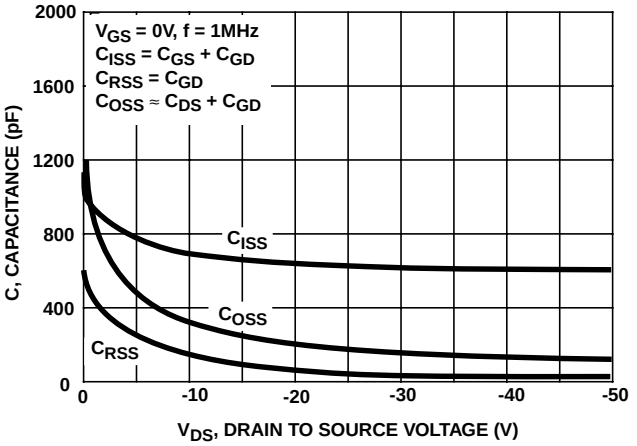


FIGURE 11. CAPACITANCE vs DRAIN TO SOURCE VOLTAGE

Typical Performance Curves Unless Otherwise Specified **(Continued)**

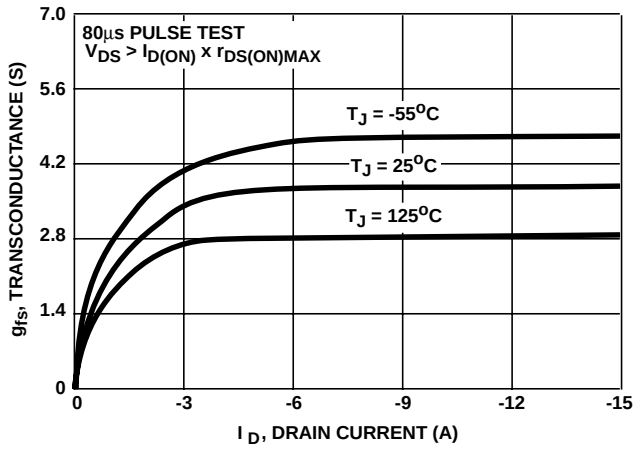


FIGURE 12. TRANSCONDUCTANCE vs DRAIN CURRENT

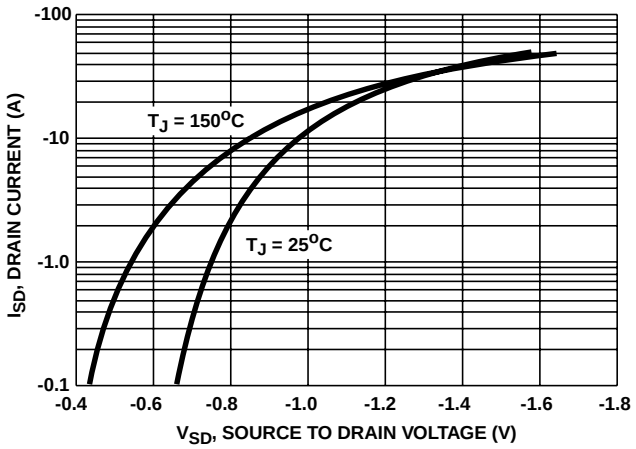


FIGURE 13. SOURCE TO DRAIN DIODE VOLTAGE

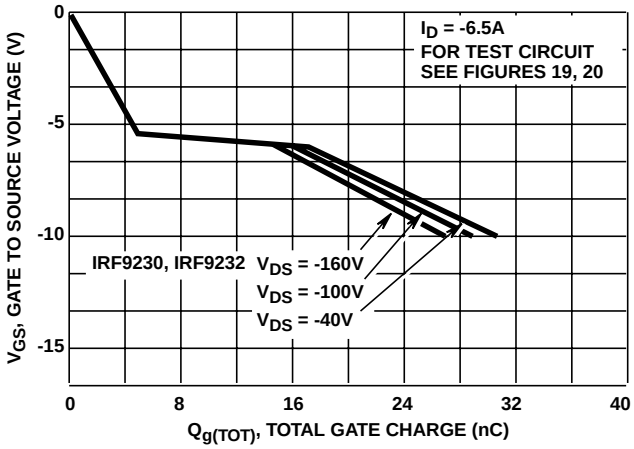


FIGURE 14. GATE TO SOURCE VOLTAGE vs GATE CHARGE

Test Circuits and Waveforms

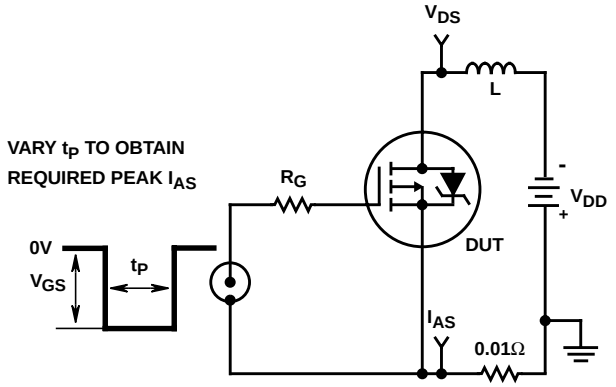


FIGURE 15. UNCLAMPED ENERGY TEST CIRCUIT

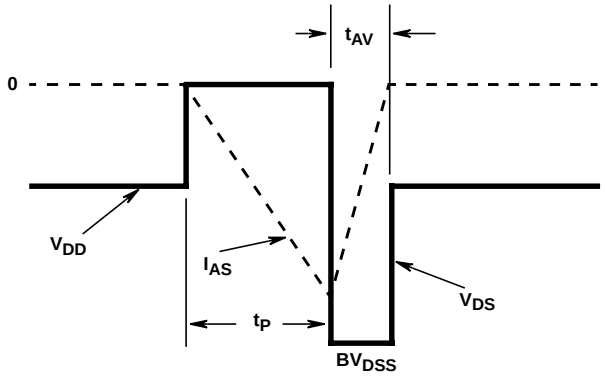


FIGURE 16. UNCLAMPED ENERGY WAVEFORMS

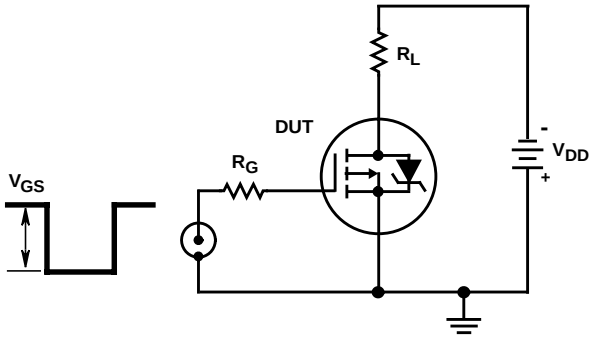


FIGURE 17. SWITCHING TIME TEST CIRCUIT

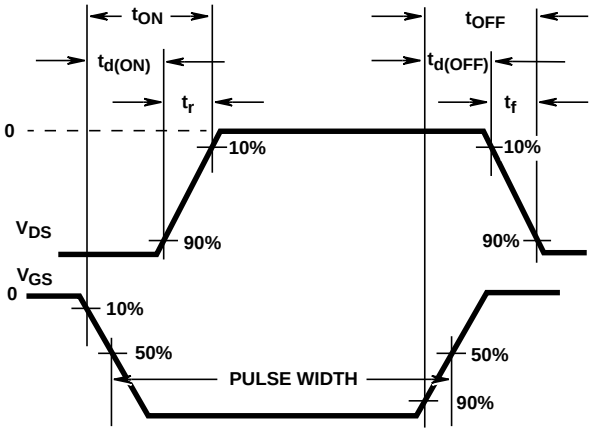


FIGURE 18. RESISTIVE SWITCHING WAVEFORMS

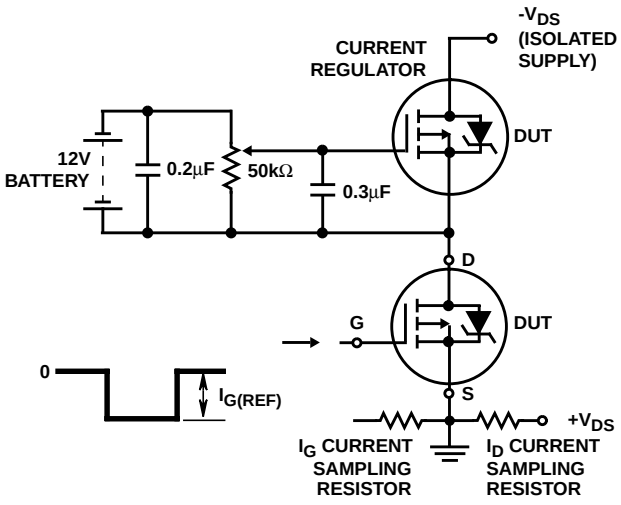


FIGURE 19. GATE CHARGE TEST CIRCUIT

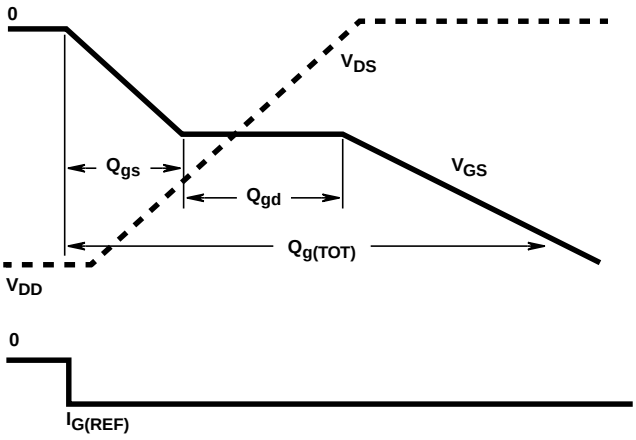


FIGURE 20. GATE CHARGE WAVEFORMS